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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PHAN, TRI H	

ART UNIT	PAPER NUMBER
2661	5

DATE MAILED: 04/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/477,217	RUSSELL ET AL.	
	Examiner	Art Unit	
	Tri H. Phan	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 17-32* is/are rejected.

7)☒ Claim(s) *12-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawing is objected to because all blocks in Fig. 1B are not labeled with descriptive legends. A proposed drawing correction or corrected drawings are required in response to this Office action. However, correction of the noted defect can be deferred until the application is allowed by the examiner.

Specification

2. The attempt to incorporate subject matter into this application by reference to "A RESOURCE MANAGEMENT PROTOCOL FOR A CONFIGURABLE NETWORK ROUTER", "METHOD AND APPARATUS FOR A REARRANGEABLY NON-BLOCKING SWITCHING MATRIX", "A METHOD FOR PATH SELECTION IN A NETWORK" and "METHOD OF PROVIDING NETWORK SERVICES" in the Cross-References to Related Applications part are improper because the US Patent Application Numbers and the filing dates are missing.

3. The attempt to incorporate subject matter into this application by reference to "GR-253: Synchronous Optical Network (SONET) Transport Systems, Common Generic Criteria, Issue 2 [Bellcore, Dec. 1995]" is improper because the copy for the reference is not received.

Claim Objections

4. Claims 1, 8, 19, 20, 21 and 28 is objected to because of the following informalities:

The limitation "a one" in Claim 1, Lines 9, 12 and 13 is not clear what it was meant by. Similar problem exists in Claim 19, Line 3; Claim 20, Lines 4 and 5; Claim 21, Line 2; Claim 28, Lines 10 and 11.

The limitation "clock/data recovery unit" in Claim 8, Line 2 is not clear what it was meant by "clock and data recovery unit" or "clock or data recovery unit".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1, 9, 18-19 and 25-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, recites the limitation "one" in lines 4 and 16.

Claim 1, recites the limitation "information stream" in line 6.

Claim 28, recites the limitation "plurality of information streams" in lines 18-19.

There is insufficient antecedent basis for these limitations in the claims.

7. Claim 9, 18-19 and 25-27 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the

elements. See MPEP § 2172.01. The omitted element "phase-locked loop" (Claim 9) in the clock and data recovery unit, "parity checker" (Claims 18 and 25), "error check entry" (Claim 19), "parity entry" (Claim 26) and "B1 byte" (Claim 27) are not disclosed in the specification nor in the drawings.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-5, 20-21 and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yoshifuji** (U.S.5,917,426) in view of **Bala et al.** (U.S.6,307,653).

- In regard to claims 1, 20-21 and 28-30, **Yoshifuji** discloses in Figs. 1-2 and 4-5 and in the respective portions of the specification that the network system ("*signal router*") includes switch network system having a plurality of switch matrices ("*switching matrices*"), which uses to control and manage connection data signals ("*information stream*") and connection data control system, wherein the switch matrix ("*switching matrix*") has a plurality of input terminals for receiving data signals ("*first number of inputs*") and a plurality of output terminals ("*second number of outputs*") formed by first through n-th link stages connected to one another through n-th sub-processing units and n-th sub-control units which are controlled by the main control unit

and main processing unit (For example see Abstract and in Fig. 1-2; Col. 1, Lines 5-17; Col. 2, Lines 16-40); a monitoring means ("*error detector*") for detecting any disorder in the connection with the interconnection data signals ("*errors in the information stream*"; For example see Col. 2, Lines 10-15) through n-th link stages mutually connected to each other, i.e. "*by virtue*", as disclosed in Col. 2, Line 58 through Col. 3, Line 6; Col. 10, Lines 7-19; a controlling means ("*controller*") for controlling the switch matrices to connect the selected input to the selected output terminals and substituting the actual path to the new one, in detection or reception of any disorder ("*receiving error information*") in the connection with the connection data signals (For example see Col. 5, Line 11 through Col. 6, Line 28). **Yoshifuji** also discloses each sub-control unit ("*controller*") connects to a corresponding switch matrix where one of a plurality of outputs connects to one of a plurality of inputs of the other switching matrices (For example see Figs. 1-2 and 4-5).

Yoshifuji fails to specially disclose the monitoring means connecting to the outputs and each controller is connected with a corresponding error detector. However, such implementation is known in the art.

For example, **Bala** discloses in Figs. 1-5 and in the respective portions of the specification that an optical matrix protection system includes NxN optical matrix switch (es) with a plurality of input and output ports, wherein each signal detector connects to each output port for in upon a failure in the connecting path and sends the switch control signals CS ("*error information*", "*command*") to the controller (For example see Fig. 3; Col. 4, Lines 47-54) and re-routing signal in upon a failure in the connecting path by connecting one of the inputs to another one of the output (For example see Col. 1, Lines 36-65; Col. 4, Lines 13-22).

Bala further discloses each one of a plurality of outputs of the first plurality of the switching matrices are coupled to a corresponding one of a plurality of inputs of the second plurality of the switching matrices (For example see Figs. 4-5).

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to use the signal detector in the optical matrix protection system as taught by **Bala** in the **Yoshifuji**'s switch network system, by implementing the signal detector at the output of the switch matrices with the motivation being to improve the ability to detect the failed path and re-route the data signal at the output of the switch matrix.

- Regarding claims 2 and 3, **Yoshifuji** further discloses the switch matrix receives the control by the sub-control unit to change the link path, i.e. "*experiences the failure*", whenever any disorder in the connection with the interconnection data signals is detected by the route search and renewal processing unit, i.e. "*identifies the error information generated by the error detector*", through the control of the main control unit (For example see Figs. 2 and 5; Col. 10, Line 29 through Col. 12, Line 22; it is obvious that each switch matrix in each of the switch link stages are mutually connected and controlled by the sub-control means which is actuated by the main control means, i.e. "*by virtue*", changes the link path when any disorder in the connection with the interconnection data signals detects by the monitoring means as disclosed in Col. 2, Lines 16-40). **Yoshifuji** fails to disclose *each of the switch matrixes is coupled to a corresponding monitoring means*. However, such implementation is known in the art.

For example, **Bala** discloses that each signal detector connects to the output port of the optical switch for monitoring the signal (For example see Fig. 3; Col. 4, Lines 47-54).

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to use the signal detector in the optical matrix protection system as taught by **Bala** in the **Yoshifuji**'s switch network system, by implementing each signal detector at each output of the switch matrix with the motivation being to improve the ability to detect the failed path and re-route the data signal at the output of each switch matrix in the system.

- In regard to claims 4 and 5, **Yoshifuji** further discloses the main switch control unit actuates the sub-switch control unit to change the connection path, i.e. "*reconfigure*", between the selected input and output of the switch matrix at each link stages by the sequence number assigned to each individual switch matrix as disclosed in Col. 8, Lines 22-31; in response to any disorder in the connection with the interconnection data signals (For example see Figs. 4-5; Col. 10, Line 29 through Col. 12, Line 22).

Bala also discloses the optical switch re-routes the link path upon the failure on the single path or failed element within the switch.

10. Claims 6-9, 22 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yoshifuji** in view of **Bala et al.** as applied to claims 1-5 above, and further in view of **Al-Salameh** (U.S.6,262,820).

- Regarding claims 6-7, **Yoshifuji** in view of **Bala** discloses the switch network system includes switch matrices with a plurality of input ports ("*optical receivers*") and output ports ("*optical transmitters*") at each switch matrix, signal detectors connecting at the output ports

("*transmitter error detector*") for monitoring the signal in upon a failure in the connecting path and supplying the switch control signals CS ("*error information*") to the controller, a main control unit managing and controlling the change of connection paths between the input and output ports of the switch matrix at each link stage. The combination of **Yoshifuji** and **Bala** fails to teach about "*the receiver error detector*" at the input port of the switch matrix. However, such implementation is known in the art.

For example, **Al-Salameh** discloses in Figs. 1-2 and 4-5 and in the respective portions of the specification that the optical node ("*signal router*"), which uses to route the transmission media ("*information stream*"), comprises a switch matrix ("*switching matrix*") having a plurality of inputs A-H for receiving transmission channel inputs ("*optical receivers*") and a plurality of outputs I-N ("*optical transmitters*") as disclosed in Col. 5, Lines 61-66; optical monitor ("*receiver error detector*") for detecting the presence or absence of input optical signal ("*errors in the information stream*") in transmission channels, i.e. "*by virtue*", generating indications and supplying the switch control signals CS ("*error information*") to the sub-controller and then to the optical switch matrix as disclosed in Col. 4, Line 66 through Col. 5, Line 12; and a main controller ("*controller*"), when receiving the CS ("*error information*"), selects an input from the plurality of inputs to an output from the plurality of outputs (For example see Figs. 4-8; Col. 5, Lines 17-37; Col. 7, Lines 23-30).

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to use the optical monitor in the optical communication system as taught by **Al-Salameh** in the **Yoshifuji** and **Bala**'s switch network system, by implementing each optical monitor at each input of the switch matrix with the motivation being to improve the

ability to detect the failed path and re-route the data signal at each input and output port of each switch matrix in the system.

- Regarding claims 8-9, 22 and 31, **Yoshifuji** further discloses the network and internal data memory ("*clock and data recovery unit*") check and backup the data signal at a predetermined period time (**Yoshifuji**: For example see Col. 4, Lines 11-17; Col. 14, Lines 39-42) when the failure detected by the signal detector at the output port is sent back, i.e. loop-back, to the main control and sub-control units for re-routing the optical signal (**Bala**: For example see Col. 3, Line 41 through Col. 4, Line 22). The combination of **Yoshifuji** and **Bala** fails to teach about "*the error counter resets and starts the error timer when reaching a terminal value*" at the input port of the switch matrix. However, such implementation is known in the art

Al-Salameh also discloses the switch matrix restores the failure by the indicating switch control SC signal set and reset ("*clearing error counter and starting error timer*") by the counter clock ("*clock and data recovery unit*") when the threshold ("*terminal value*") has been reached as disclosed in Fig. 9; Col. 9, Line 34 through Col. 10, Line 16; and the add/drop multiplexer ("*demultiplexer*") as disclosed in Figs. 2 and 12; Col. 4, Line 17 through Col. 5, Line 60.

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to use the counter clock in the optical communication system as taught by **Al-Salameh** in the **Yoshifuji** and **Bala**'s switch network system, by implementing the counter clock in the **Yoshifuji** and **Bala**'s switch network system with the motivation being to improve the ability to detect the failed path and re-route the data signal at a predetermined time and value in the system.

11. Claims 10-11, 17-19, 23-27 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yoshifuji** in view of **Bala et al.** as applied to claims 1-5 above, and further in view of **Maezawa et al** (U.S.6,145,024).

- Regarding claims 10-11, 17-19, 23-27 and 32, **Yoshifuji** in view of **Bala** discloses the switch network system includes switch matrices with a plurality of input ports ("*optical receivers*") and output ports ("*optical transmitters*") at each switch matrix, signal detectors ("*error checkers*") connecting at the output ports for monitoring the signal in upon a failure in the connecting path and supplying the switch control signals CS ("*error information*") to the controller, a main control unit managing and controlling the change of connection paths between the input and output ports of the switch matrix at each link stage. The combination of **Yoshifuji** and **Bala** fails to teach about "*the frame circuit*". However, such implementation is known in the art.

For example, **Maezawa** discloses in Figs. 1-5 and in the respective portions of the specification that the switching matrix device with a plurality of switching ports for transferring data in multiplex channel path mode or high speed single channel path mode of optical fiber link with optical fiber frames, i.e. "*SONET frames*" (For example see Fig. 1 and 5; it is obvious that the frames are received in a "*sequence*"), wherein the link connection control circuit detects the error such as CRC, connection or frame validity error ("*framing error*") through the SOF ("*start-of-frame*") and EOF ("*end-of-frame*") which use for the purpose of connection control (For example see Fig. 5; Col. 16, Line 21 through Col. 17, Line 5); and compares ("*comparing*") with

relevant channel path as disclosed in Col. 7, Line 13-18; Col. 23, Lines 9-26; or with reserved bits in PCONF, i.e. "*B1 byte in parity entry*" (For example see Fig. 6; Col. 22, Lines 1-31) and sends the control signal ("*error information*") to the channel path control circuit for link recovery operations from error detections (For example see Figs. 2-4; Col. 14, Lines 21-54; Col. 18, Line 26 through Col. 19, Line 17).

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to use the frame circuit in the optical communication system as taught by **Maezawa** in the **Yoshifuji** and **Bala**'s switch network system, by implementing the frame circuit in the **Yoshifuji** and **Bala**'s switch network system with the motivation being to improve the ability to detect the errors of the optical frames in the multiplex channel path or high speed single channel path mode.

Allowable Subject Matter

12. Claims 12-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Many references in the art disclose system and method for isolating faults in the switch matrix, but none of those references disclose or suggest the combination of limitations specified in the independent claims including the integrator configured to determine and calculate the error rate based on error count during a period of time.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Lindberg et al. (U.S.6,088,329), **Maddern et al.** (U.S.5,610,928) and **Zwan et al.** (U.S.5,991,270) are all cited to show devices and methods for improving the fault tolerant technique in the communication architectures which are considered pertinent to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tri H. Phan whose telephone number is (703)305-7444. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Douglas W. Olms can be reached on (703)305-4703.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703)872-9314

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703)305-3900.

DANG TON
PRIMARY EXAMINER

Tri H. Phan
April 20, 2003